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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,600	09/16/2005	Uwe Guenther	10191/4126	9491
26646	7590 11/15/2006		EXAMINER	
KENYON & KENYON LLP			WILLIAMS, HOWARD L	
ONE BROADWAY NEW YORK, NY 10004			ART UNIT	PAPER NUMBER
			2819 DATE MAILED: 11/15/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	A multiple makes	_			
Office Action Summary		Application No.	Applicant(s)				
		10/519,600	GUENTHER ET AL.				
		Examiner	Art Unit	_			
		Howard L. Williams	2819				
Period fo	The MAILING DATE of this communication ap or Reply	opears on the cover sheet with the c	orrespondence address				
WHIC - Exter after - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR REP CHEVER IS LONGER, FROM THE MAILING It asions of time may be available under the provisions of 37 CFR 1 SIX (6) MONTHS from the mailing date of this communication. Period for reply is specified above, the maximum statutory period re to reply within the set or extended period for reply will, by statute eply received by the Office later than three months after the mailined and patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNICATION .136(a). In no event, however, may a reply be tind d will apply and will expire SIX (6) MONTHS from tte, cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status							
1)[]	Responsive to communication(s) filed on 29.	August 2006					
		is action is non-final.					
	Since this application is in condition for allow		esecution as to the merits is				
٠,٣	closed in accordance with the practice under						
Dispositi	on of Claims	, , , , , , , , , , , , , , , , , , , ,					
	Claim(s) 9-16 is/are pending in the applicatio	n					
	4a) Of the above claim(s) is/are withdrawn from consideration.						
	Claim(s) is/are allowed.						
·	Claim(s) <u>——</u> is/are allowed.  Claim(s) <u>9-16</u> is/are rejected.						
	Claim(s) is/are objected to.						
	Claim(s) are subject to restriction and/	or election requirement					
		or election requirement.					
	on Papers						
9) The specification is objected to by the Examiner.							
10)	10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
	Applicant may not request that any objection to the	e drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).				
_	Replacement drawing sheet(s) including the corre		•				
11)[_]	The oath or declaration is objected to by the E	Examiner. Note the attached Office	Action or form PTO-152.				
Priority u	ınder 35 U.S.C. § 119						
a)[	Acknowledgment is made of a claim for foreig  All b) Some * c) None of:  1. Certified copies of the priority documer  2. Certified copies of the priority documer  3. Copies of the certified copies of the pri application from the International Bures see the attached detailed Office action for a lis	nts have been received. nts have been received in Applicati ority documents have been receive au (PCT Rule 17.2(a)).	on No ed in this National Stage				
Attachmen 1) ⊠ Notic	t(s) e of References Cited (PTO-892)	4) 🔲 Interview Summary	(PTO-413)				
2) 🔲 Notic	e of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail D	ate				
	nation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date	5)  Notice of Informal F 6)  Other:	atent Application				

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. (US 20010044862 A1). Mergard discloses a method for serially transmitting data between a first station (406; fig. 4) and second station (418; fig. 4). Mergard provides the serial transmission to free up pins (para 0008). The serial-to-parallel converters and parallel-to-serial converters are labeled simply converters in figure 4 (202D, 202F) but are shown with a parallel input and serial output for 202D so it receives at least two signals and serially transmits these signals to the second station (418). Mergard does not disclose the serial-to-parallel converter and parallel-to-serial converter as shift registers. However, shift registers are well known for that purpose and the use of shift registers configured to provide parallel-to-serial conversion and vice-versa would have been obvious to one of ordinary skill in the art.

Mergard discloses a system with embedded controllers. In figure 1 the processor is element 100 and figure 2 discloses the bus controller and additionally includes a serial bus controller. Mergard thus appears to not load the processor 100.

Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada (JP 11-178349 A). Shimada discloses two stations with serial transmission between them to reduce the to reduce the number of transmission lines for transferring the gate signals. The clock circuit is 11. The serial-to-parallel and parallel-to-serial converters are 12 and 14. Yamada does not discuss the clock rate in the abstract but it would have been obvious to select a clock of sufficient speed such that bits would not be missed. Yamada also does not disclose the serial-to-parallel and parallel-to-serial converters as shift registers however it is considered that it would have been obvious to one of ordinary skill that shift registers are commonly used for this purpose.

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The response does not appear to even address the rejection above. See 37 CFR 1.111(b) and MPEP 714.02.

Claims 9-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US 5475831 A). Yoshida discloses a serial transmission system that includes a shift register for the serialization/deserialization function and is driven by the clocking circuitry. It is fed from the buffer which provides isolation between the CPU and the serializer such that the CPU does not need to directly control the serialization. The Yoshida discloses that this arrangement reduces the load on the CPU (col.4 line 1) so it would have been obvious that the serializer transmits without loading the CPU.

Applicants' response filed 29 August 2006 has been fully considered but it is not persuasive. Any particular points raised are believed to have been addressed above.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Thomsen et al (US 5475854 A) discloses serialized bus to reduce the pin count on a chip. AMD/Bell (WO 98/45787) discloses pin count reduction through serial transmission.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office central facsimile number for application specific correspondence intended for entry is 571-273-8300.

11/8/06

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Howard L. Williams Primary Examiner Art Unit 2819